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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,999	02/16/2001	Jay E. Uglow	LAMP1P106A	2171

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EXAMINER	
PHAM, THANHHA S	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/785,999	UGLOW ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action responses to Applicant's Amendment in Paper No. 15 dated 11/25/02.

Claim Rejections - 35 USC § 102

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 1-4, 7-12 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al [US 6,211,063].

Liu et al, figs 3-10 and col 1-6, discloses the claimed method for making a multi-layer inter-metal dielectric over a substrate thereby forming a dielectric structure for dual-damascene application comprising steps of:

forming a barrier layer (35, a silicon nitride, fig 3) on a substrate (30/34/32) and metallization lines (32) within the substrate;

forming an inorganic dielectric silicon dioxide layer (36, FSG, fig 4, col 4 lines 13-19) to define a via dielectric layer over the barrier layer, the inorganic dielectric layer being highly selective relative to the barrier layer when etched;

forming a carbon-doped oxide layer (46, organic HSQ, fig 6, col 4 lines 48-57 and col 3 lines 24-26) to define a trench dielectric layer over the inorganic dielectric silicon dioxide layer;

forming a trench through the interlayer dielectric film by a first etch chemistry (fig 8, col 5 lines 4-49); and

forming a via (fig 9, col 5 lines 50-67 and col 6 lines 1-10) in the trench extending through inorganic dielectric silicon dioxide layer to the barrier layer by a second etch chemistry, the second etch chemistry being different than the first etch chemistry.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith [US 6,277,733] in view of Usami [US 6,077,574].

Smith , figs 1-2's and col 1-5, discloses a method for making a multi-layer inter-metal dielectric over a substrate thereby forming a dielectric structure for dual-damascene application comprising steps of:

forming a barrier layer (422, a silicon nitride, fig 2a) on a substrate and metallization lines (420) within the substrate;

forming an inorganic dielectric silicon dioxide layer (424, FSG or silicon dioxide by TEOS, fig 2a , col 3 lines 25-27) to define a via dielectric layer over the barrier layer, the inorganic dielectric layer being highly selective relative to the barrier layer when etched;

forming an interlayer dielectric film (430, fig 2c) to define a trench dielectric layer over the inorganic dielectric silicon dioxide layer;

forming a trench through the interlayer dielectric film by a first etch chemistry;

forming a via in the trench extending through inorganic dielectric silicon dioxide layer to the barrier layer by a second etch chemistry (see col 3 lines 63-67 and col 4 lines 1-7);

etching the barrier layer (col 4 lines 49-52);

forming a via and trench barrier layer (434, fig 2g) to cover a surface within the via and the trench wherein the via and trench barrier layer is one of tantalum nitride material and tantalum material.

Smith does not expressly teach forming said interlayer dielectric film by a carbon doped oxide layer.

However, Usami teaches using the carbon-doped oxide layer would provide a better interlayer dielectric film with a low dielectric constant of about and no great than 3 and a good resistance to moisture and heat.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Usami to the process of Smith to use the carbon-doped oxide layer for the interlayer dielectric film to define the trench dielectric layer for forming the trench in the

dual damascene application. By doing so, a better device with better interconnection of low RC and good resistance to moisture & heat would be formed.

With respect to claim 3 and 14, those skilled in the art should recognize that the second etch chemistry for etching the carbon-doped oxide would be different to the first etch chemistry for etching the silicon dioxide for by TEOS or FSG in the process of Smith in view of Usami.

2. Claims 1-4 and 7-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al [US 6,255,735] in view of Usami [US 6,077,574].

Wang et al, figs 1-11 and col 1-8, discloses a method for making a multi-layer inter-metal dielectric layer over a substrate thereby forming a dielectric structure for dual-damascene application comprising steps of:

forming a barrier layer (12, silicon nitride , fig 1) on a substrate and metallization lines within the substrate;

forming an inorganic dielectric silicon dioxide layer (14, silicon dioxide or SiOF, fig 2, col 5 lines 40-41) to define a via dielectric layer over the barrier layer, said inorganic dielectric silicon dioxide being highly selective to the barrier layer when etched;

forming an interlayer dielectric film (18, fig 3, col 5 lines 51-67 and col 6 lines 1-11) to define a trench dielectric layer over the inorganic dielectric silicon dioxide layer;

forming a trench through the interlayer dielectric film by implementing a first etch chemistry; and

forming a via in the trench extending through the inorganic dielectric silicon dioxide layer through the insulating by implementing a second etch chemistry which is selective to the barrier layer wherein the second etch chemistry is different than the first etch chemistry.

[see figs 8-9, col 6 lines 35-63].

Wang does not expressly teach forming said interlayer dielectric film by using a carbon doped oxide layer.

Usami teaches using the carbon-doped oxide layer would provide the interlayer dielectric film with a low dielectric constant of about and no great than 3 and a good reistance to moisture and heat.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Usami to the process of Wang et al to use the carbon-doped oxide layer as being claimed to define the trench dielectric layer to form the trench for interconnection in a device with low RC, good reistance to moisture and resistance to heat. By doing so, a better device with better reliable performance will be formed.

3. Claims 5-7 and 12-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al [US 6,255,735] in view of Usami [US 6,077,574] as applied to claims 3, 4 or 11 above, in further view of Wolf et al ["Silicon Processing for VLSI Era Vol 1: Process Technology" Lattice Press 1986, pp 194] as submitted by IDS.

Wang et al in view of Usami substantially discloses the claimed method including forming the inorganic dielectric silicon dioxide layer (14) a via dielectric layer over the barrier layer, said inorganic dielectric silicon dioxide being highly selective to the barrier

layer when etched. Wang et al in view of Usami does not expressly teach forming said inorganic dielectric silicon dioxide layer by TEOS.

However, it has been known in the art that TEOS can be used for the inorganic silicon dioxide layer. See Wolf et al as an evidence that shows using TEOS for forming inorganic silicon dioxide layer. Therefore, it would have been obvious for those skilled in the art to select TEOS as a known material for forming the inorganic dielectric silicon dioxide in the process of Wang et al in view of Usami. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945). Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig - saw puzzle (Id. at 301.)

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al [US 6,255,735] in view of Usami [US 6,077,574] as applied to claim 10 above, and further in view of Smith [US 6,277,733].

Wang et al in view of Usami substantially discloses the claimed method except teaching forming a via and trench barrier layer to cover a surface within the via and the trench wherein the via and trench barrier layer is one of tantalum nitride material and tantalum material.

Smith teaches forming the via and trench barrier layer (434, fig 2g) of Ta/TaN to cover the surface of the via and the trench of the dual damascene structure (429).

It would have been obvious for those skilled in art, in view of Smith, to form the via and trench barrier layer of tantalum or tantalum nitride as being claimed in the process of Wang et al in view of Usami to make a better device with a better interconnection wherein the peeling and interdiffusion problems are prevented.

Response to Arguments

5. Applicant's arguments filed 11/25/02 have been fully considered but they are not persuasive.

In response to Applicant's argument that "**Usami teaches a fluorine and carbon doped silicon oxide dielectric film.... the properties of a fluorine and carbon doped dielectric are fundamentally different than a carbon doped oxide layer as claimed by Applicant..... Usami teaches away from the present invention... Therefore, the Office has failed to establish a prima facies case of obviousness**", the argument is not persuasive because Usami suggests advantage of using a carbon-doped oxide (as being claimed – "forming a carbon-doped oxide layer") even though with combination of fluorine and carbon in the doped silicon oxide dielectric film. It still is obvious for those skilled in the art to combine the teaching of Usami to the process of Smith or Wang et al to use the carbon-doped oxide layer for forming the interlayer dielectric film with low dielectric constant layer and good resistance to moisture and heat.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-

6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
December 26, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800